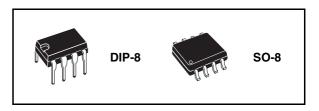


### High-voltage high and low side driver

#### **Features**

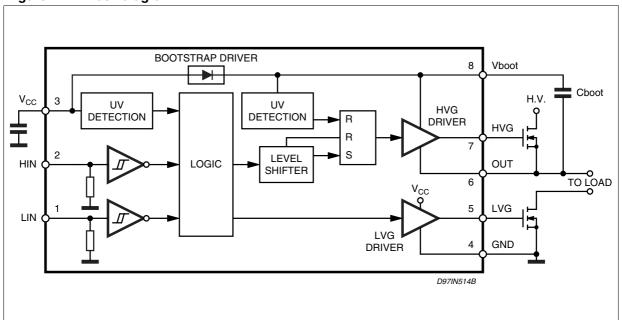
- High voltage rail up to 600V
- dV/dt immunity ±50V/nsec in full temperature range
- Driver current capability:
  - 400mA source,
  - 650mA sink
- Switching times 50/30 nsec rise/fall with 1nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull down
- Under voltage lock out on lower and upper driving section
- Internal bootstrap diode
- Outputs in phase with inputs



#### **Description**

The L6385E is an high-voltage device, manufactured with the BCD"OFF-LINE" technology. It has an Half - Bridge Driver structure that enables to drive independent referenced N Channel Power MOS or IGBT. The High Side (Floating) Section is enabled to work with voltage Rail up to 600V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.





Contents L6385E

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L6385E Electrical data

## 1 Electrical data

#### 1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>out</sub>	Output voltage	-3 to V <sub>boot</sub> -18	V
V <sub>cc</sub>	Supply voltage	- 0.3 to +18	V
$V_{boot}$	Floating supply voltage	-1 to 618	V
V <sub>hvg</sub>	High sidegate output voltage	-1 to V <sub>boot</sub>	V
$V_{lvg}$	Low side gate output voltage	-0.3 to V <sub>cc</sub> +0.3	V
$V_{i}$	Logic input voltage	-0.3 to $V_{cc}$ +0.3	V
dV <sub>out</sub> /d <sub>t</sub>	Allowed output slew rate	50	V/ns
P <sub>tot</sub>	Total power dissipation (T <sub>J</sub> = 85 °C)	750	mW
T <sub>j</sub>	Junction temperature	150	°C
T <sub>s</sub>	Storage temperature	-50 to 150	°C

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

#### 1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
R <sub>th(JA)</sub>	Thermal Resistance Junction to ambient	150	100	°C/W

## 1.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit
$V_{out}$	6	Output voltage		(1)		580	V
V <sub>BS</sub> (2)	8	Floating supply voltage		(1)		17	V
f <sub>sw</sub>		Switching frequency	HVG,LVG load C <sub>L</sub> = 1nF			400	kHz
V <sub>cc</sub>	3	Supply voltage				17	V
T <sub>J</sub>		Junction temperature				125	ç

<sup>1.</sup> If the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V

<sup>2.</sup>  $V_{BS} = V_{boot} - V_{out}$ 

Pin connection L6385E

## 2 Pin connection

Figure 2. Pin connection (Top view)

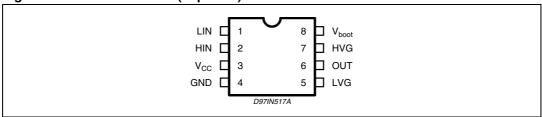


Table 4. Pin description

N°	Pin	Туре	Function			
1	LIN	I	Low side driver logic input			
2	HIN	I	High side driver logic input			
3	V <sub>cc</sub>		Low voltage power supply			
4	GND		Ground			
5	LVG (1)	0	Low side driver output			
6	VOUT	0	High side driver floating reference			
7	HVG <sup>(1)</sup>	0	High side driver output			
8	V <sub>boot</sub>		Bootstrap supply voltage			

<sup>1.</sup> The circuit guarantees 0.3V maximum on the pin (@ Isink = 10mA). This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

## 3 Electrical characteristics

## 3.1 AC operation

Table 5. AC operation electrical characteristcs  $(V_{CC} = 15V; T_J = 25^{\circ}C)$ 

Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit
t <sub>on</sub>		High/low side driver turn-on propagation delay	V <sub>out</sub> = 0V		110		ns
t <sub>off</sub>	1 vs 5 2 vs 7	High/low side driver turn-off propagation delay	V <sub>out</sub> = 0V		105		ns
t <sub>r</sub>	5, 7	Rise time	C <sub>L</sub> = 1000pF		50		ns
t <sub>f</sub>	5, 7	Fall time	C <sub>L</sub> = 1000pF		30		ns

## 3.2 DC operation

**Table 6.** DC operation electrical characteristcs  $(V_{CC} = 15V; T_J = 25^{\circ}C)$ 

Symbol	Pin	Parameter	Test condition	Min	Тур	Max	Unit	
Low supply voltage section								
V <sub>cc</sub>		Supply voltage				17	V	
V <sub>ccth1</sub>		Vcc UV turn on threshold		9.1	9.6	10.1	V	
V <sub>ccth2</sub>		Vcc UV turn off threshold		7.9	8.3	8.8	V	
V <sub>cchys</sub>		Vcc UV hysteresis			1.3		V	
I <sub>qccu</sub>	3	Undervoltage quiescent supply current	$V_{cc} \le 9V$		150	220	μА	
I <sub>qcc</sub>		Quiescent current	V <sub>in</sub> = 15V		250	320	μА	
R <sub>dson</sub>		Bootstrap driver on resistance <sup>(1)</sup>	V <sub>cc</sub> ≥12.5V		125		Ω	
Bootstra	pped	supply voltage section						
$V_{BS}$		Bootstrap supply voltage				17	V	
V <sub>BSth1</sub>		V <sub>BS</sub> UV turn on threshold		8.5	9.5	10.5	V	
V <sub>BSth2</sub>		V <sub>BS</sub> UV turn off threshold		7.2	8.2	9.2	V	
V <sub>BShys</sub>	8	V <sub>BS</sub> UV hysteresis			1.3		V	
I <sub>QBS</sub>		V <sub>BS</sub> quiescent current	HVG ON			200	μА	
I <sub>LK</sub>		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 600V$			10	μА	
High/low	side (	driver						
I <sub>so</sub>	F 7	Source short circuit current	$V_{IN} = V_{ih} (t_p < 10 \mu s)$	300	400		mA	
I <sub>si</sub>	5,7	Sink short circuit current	$V_{IN} = V_{il} (tp < 10 \mu s)$	450	650		mA	

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Electrical characteristics L6385E

iable 0.	be operation electrical characteristics (continued)( $v_{CC} = 15v$ , $v_{J} = 25v$						3 C)
Symbol	Pin	Parameter	Тур	Max	Unit		
Logic inp	outs						
V <sub>il</sub>	1, 2	Low level logic threshold voltage				1.5	V
$V_{ih}$	1, 2	High level logic threshold voltage		3.6			V
I <sub>ih</sub>	1, 2	High level logic input current	V <sub>IN</sub> = 15V		50	70	μΑ
I <sub>il</sub>	1, 2	Low level logic input current	V <sub>IN</sub> = 0V			1	μΑ
1 0	:- 11	ad in the fall accions access					

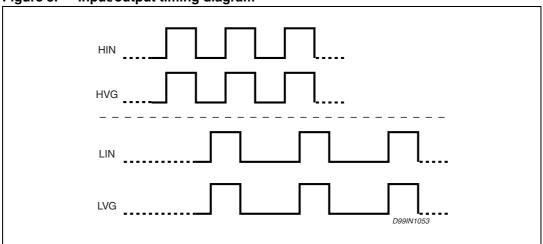
**Table 6.** DC operation electrical characteristcs (continued)( $V_{CC} = 15V$ ;  $T_J = 25^{\circ}C$ )

$$\mathsf{R}_{\mathsf{DSON}} = \frac{(\mathsf{V}_{\mathsf{CC}} - \mathsf{V}_{\mathsf{CBOOT1}}) - (\mathsf{V}_{\mathsf{CC}} - \mathsf{V}_{\mathsf{CBOOT2}})}{\mathsf{I}_{1}(\mathsf{V}_{\mathsf{CC}}, \mathsf{V}_{\mathsf{CBOOT1}}) - \mathsf{I}_{2}(\mathsf{V}_{\mathsf{CC}}, \mathsf{V}_{\mathsf{CBOOT2}})}$$

where  $I_1$  is pin 8 current when  $V_{CBOOT} = V_{CBOOT1}$ ,  $I_2$  when  $V_{CBOOT} = V_{CBOOT2}$ 

## 3.3 Timing diagram





<sup>1.</sup> R<sub>DS(on)</sub> is tested in the following way:

L6385E Bootstrap driver

#### 4 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4* a). In the L6385E a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 4* b. An internal charge pump (*Figure 4* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

#### 4.1 C<sub>BOOT</sub> selection and charging

To choose the proper  $C_{BOOT}$  value the external MOS can be seen as an equivalent capacitor. This capacitor  $C_{EXT}$  is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors  $C_{\text{EXT}}$  and  $C_{\text{BOOT}}$  is proportional to the cyclical voltage loss. It has to be:

e.g.: if  $Q_{gate}$  is 30nC and  $V_{gate}$  is 10V,  $C_{EXT}$  is 3nF. With  $C_{BOOT}$  = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the  $C_{BOOT}$  selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than  $200\mu A$ , so if HVG  $T_{ON}$  is 5ms,  $C_{BOOT}$  has to supply  $1\mu C$  to  $C_{EXT}$ . This charge on a  $1\mu F$  capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if  $V_{OUT}$  is close to GND (or lower) and in the meanwhile the LVG is on. The charging time ( $T_{charge}$ ) of the  $C_{BOOT}$  is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS  $R_{DSON}$  (typical value: 125  $\Omega$ ). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where  $Q_{gate}$  is the gate charge of the external power MOS,  $R_{dson}$  is the on resistance of the bootstrap DMOS, and  $T_{charge}$  is the charging time of the bootstrap capacitor.

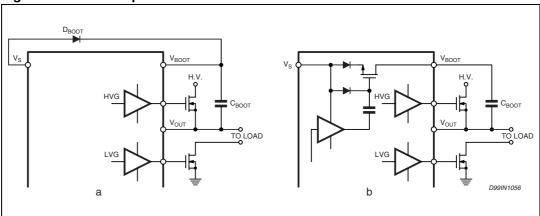
Bootstrap driver L6385E

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the  $T_{charge}$  is  $5\mu s$ . In fact:

$$V_{drop} \,=\, \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

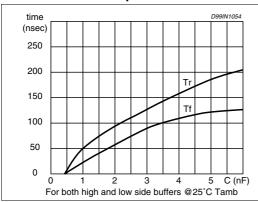
 $V_{drop}$  has to be taken into account when the voltage drop on  $C_{BOOT}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap driver



## 5 Typical characteristic

Figure 5. Typical rise and fall times vs Figure 6. Quiescent current vs supply load capacitance voltage



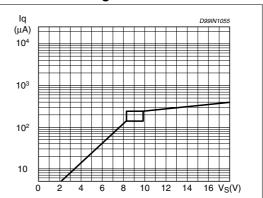
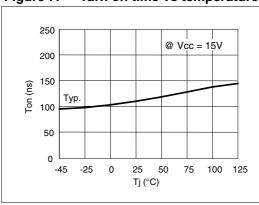


Figure 7. Turn on time vs temperature Figure 8. Turn Off time vs temperature



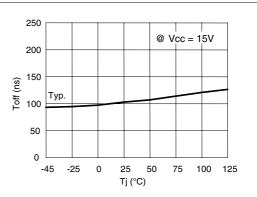
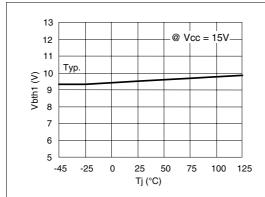
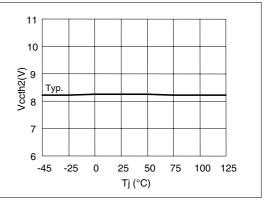


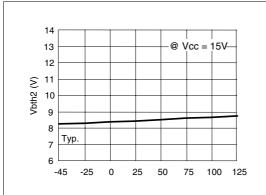
Figure 9. VBOOT UV turn On threshold Figure 10. Vcc UV turn Off threshold vs vs temperature temperature





Typical characteristic L6385E

Figure 11. V<sub>BOOT</sub> UV turn Off threshold Figure 12. Output source current vs vs temperature temperature



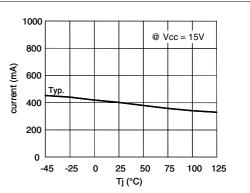
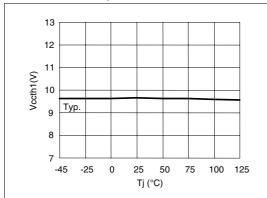
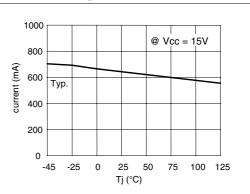


Figure 13. Vcc UV turn On threshold vs Figure 14. Output sink current vs temperature temperature





## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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Figure 15. DIP-8 mechanical data and package dimensions

DIM.		mm			inch		OUTLINE AND
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	OUTLINE AND MECHANICAL DATA
Α		3.32			0.131		
a1	0.51			0.020			
В	1.15		1.65	0.045		0.065	
b	0.356		0.55	0.014		0.022	
b1	0.204		0.304	0.008		0.012	
D			10.92			0.430	
Е	7.95		9.75	0.313		0.384	
е		2.54			0.100		U
еЗ		7.62			0.300		
e4		7.62			0.300		
F			6.6			0.260	
I			5.08			0.200	
L	3.18		3.81	0.125		0.150	DIP-8
Z			1.52			0.060	
		Z	b -	B e3	B1 e	Z	e4  b1
			8	D	5		

Figure 16. SO-8 mechanical data and package dimensions

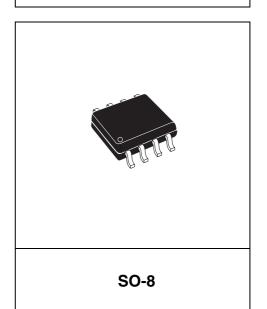
DIM.		mm		inch		
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
С	0.170		0.230	0.0067		0.0091
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
Е	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1 <sup>(2)</sup>	3.800	3.900	4.000	0.1496	0.1535	0.1575
е		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

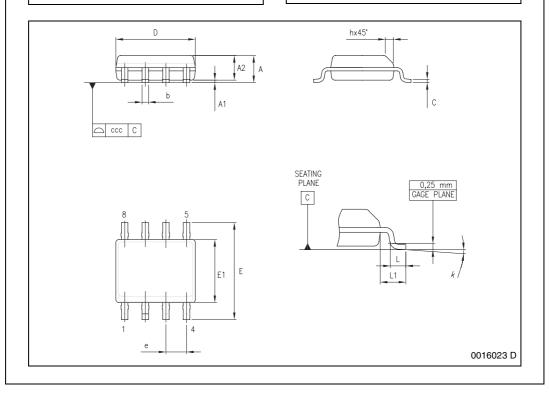
Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs.

Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).

2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

#### **OUTLINE AND MECHANICAL DATA**





Order codes L6385E

## 7 Order codes

Table 7. Order codes

Part number	Package	Packaging
L6385E	DIP-8	Tube
L6385ED	SO-8	Tube
L6385ED013TR	SO-8	Tape and reel

L6385E Revision history

# 8 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Oct-2007	1	First release

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